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13JUL00 E552510-2 D00528
P01/7700 0.00-0017158.7

The Patent Office
Cardiff Road
Newport
Gwent NP9 1RH

1. Your reference

GBP13468A

2. Patent application number
(The Patent Office will fill in this part)

0017158.7

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

Seiko Epson Corporation
4-1, Nishishinjuku 2-chome
Shinjuku-ku
Tokyo 163-0811
Japan

Patents ADP number *(if you know it)*

712331003

If the applicant is a corporate body, give the country/state of its incorporation

Tokyo, Japan

4. Title of the invention

THIN-FILM SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

5. Name of your agent *(if you have one)*

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

Miller Sturt Kenyon
9 John Street
London WC1N 2ES
United Kingdom

Patents ADP number *(if you know it)*

07395486001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

Yes

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Satoshi INOUE et al.

Application No.: 09/899,058

Filed: July 6, 2001 Docket No.: 110041

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

CLAIM FOR PRIORITY

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

The benefit of the filing date of the following prior foreign application filed in the following foreign country is hereby requested for the above-identified patent application and the priority provided in 35 U.S.C. §119 is hereby claimed:

United Kingdom Patent Application No. 0017158.7 filed on July 11, 2000.

In support of this claim, a certified copy of said original foreign application:

__X__ is filed herewith.

_____ was filed on _____ in Parent Application No. _____ filed _____.

_____ will be filed at a later date.

It is requested that the file of this application be marked to indicate that the requirements of 35 U.S.C. §119 have been fulfilled and that the Patent and Trademark Office kindly acknowledge receipt of this document.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Thomas J. Pardini
Registration No. 30,411

JAO:TJP/zmc

Date: October 22, 2001

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I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation and Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein together with the Statement of inventorship and of right to grant of a Patent (Form 7/77), which was subsequently filed.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

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Signed

Dated - 3 AUG 2001

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Continuation sheets of this form	
Description	8
Claim(s)	3
Abstract	1
Drawing(s)	7 + 7

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	
Request for preliminary examination and search *(Patents Form 9/77)*	1
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature: Miller Sturt Kenyon — Date: 11th July 2000

12. Name and daytime telephone number of person to contact in the United Kingdom: C M Sturt 020 7242 5974

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

Notes

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Patents Form 7/77

Patents Act 1977
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The Patent Office

7/77

Statement of inventorship and of right to grant of a patent

The Patent Office

Cardiff Road
Newport
Gwent NP9 1RH

1. Your reference

GBP13468A

2. Patent application number
(If you know it)

0017158.7

3. Full name of the or of each applicant

Seiko Epson Corporation

4. Title of the invention

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

5. State how the applicant(s) derived the right from the inventor(s) to be granted a patent

by virtue of employment

6. How many, if any, additional Patents Forms 7/77 are attached to this form?
(see note (c))

7. I/We believe that the person(s) named over the page *(and on any extra copies of this form)* is/are the inventor(s) of the invention which the above patent application relates to.

Signature

Miller Sturt Kenyon

Date

10/07/01

8. Name and daytime telephone number of person to contact in the United Kingdom

C M Sturt 020 7242 5974

Notes

a) If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.

b) Write your answers in capital letters using black ink or you may type them.

c) If there are more than three inventors, please write the names and addresses of the other inventors on the back of another Patents Form 7/77 and attach it to this form.

d) When an application does not declare any priority, or declares priority from an earlier UK application, you must provide enough copies of this form so that the Patent Office can send one to each inventor who is not an applicant.

Patents Form 7/77

Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

INOUE Satoshi
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Patents ADP number *(if you know it)*: 81568270001

Patents ADP number *(if you know it)*:

Reminder

THIN-FILM SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

FIELD OF THE INVENTION

The present invention relates to a thin-film semiconductor device and the method of manufacture and, particularly, relates to a thin-film semiconductor device having memory functions by the application of a low-temperature polysilicon TFT (thin-film transistor) and the method of manufacture thereof.

PRIOR ART

As one type of nonvolatile memory, a floating gate nonvolatile memory is conventionally known. This memory demonstrates nonvolatile memory functions by injecting carriers to a floating gate and holding therein.

With this type of nonvolatile memory, the floating gate EPROM at a p-channel having an MOS structure was first used for practical purposes. For this type of floating gate, polycrystalline silicon doped with a large quantity of impurities is used, and carriers are injected to floating gates (for writing or programming) by causing avalanche breakdown at drain junctions. This type of nonvolatile memory is called FAMOS (Floating-gate Avalanche-injection MOS). The information written in FAMOS can be erased by the irradiation of ultraviolet rays and X-rays at a sufficiently high energy level.

Nonvolatile memory, having a structure wherein a control gate made of polycrystalline silicon is laminated on the FAMOS floating gate, is called SAMOS (Stacked-gate Avalanche-injection MOS) memory. An appropriate level of voltage is applied to the control gate during the injection process of carriers for avalanche breakdown, so that an electric field near a drain is intensified and avalanche breakdown is likely to occur. At the same time, the electrons generated by the avalanche breakdown may be more effectively attracted to the side of a floating gate, thereby shortening the writing time. Additionally, the control gate may be used like the gate electrodes of normal MOS transistors during the process of

information readout.

Devices having an SAMOS structure at an n-channel have been recently referred to as FAMOS, and have become the standard EPROM structure. In this case, channel hot electrons are injected into a floating gate.

Furthermore, according to other research, MOS memory has been proposed as in the thesis, "MOS Memory Using Germanium Nanocrystals Formed by Thermal Oxidation of Sil-xGex, Ya-Chin King et al., IEDM 98 115-118." This is a memory element in which a charge trapping bodies comrising germanium fine particles are buried in an MOSFET gate insulating body. On the other hand, since economical glass substrates, instead of expensive quartz substrates, may be used and preferable TFT characteristics may be easily obtained, the polysilicon TFT formed in the process of a relatively low temperature (about 600°C or below) has been focused upon.

However, although this TFT is used for the picture elements of displays and peripheral circuits, it is not a device that could be used as a memory element like the above-noted MOS memory. Therefore, a memory and a display cannot be mounted on one panel in one body in, for example, an active matrix display in which a TFT is used for a picture element unit. This is one of the obstacles to the further miniaturization and electricity reduction of liquid crystal display devices or the like.

DISCLOSURE OF THE INVENTION

It is an object of the present invention to provide memory functions to a thin-film transistor (TFT) element and to broaden the application of TFT elements.

In order to achieve the above objective, a thin-film semiconductor device according to the present invention has a substrate, a semiconductor layer, in which each source, channel and drain region is formed on the substrate, and an insulating film is formed on the semiconductor layer, and granular electron trapping bodies are placed inside the insulating film to trap the electrons of injected carriers.

Preferably, the electron trapping bodies are a plurality of semiconductor or

metal granules. For instance, the plurality of granules is made up of silicon particles. It is preferable that these silicon particles have a diameter of 1 μm or less, 1000 angstroms or less, or 500 angstroms or less.

Moreover, it is preferable that the insulating film comprise a first insulating film formed on the semiconductor layer and a second insulating film formed on the first insulating film, with the plurality of granules being placed between the first insulating film and the second insulating film. In this case, the first insulating film is preferably formed at an extremely thin thickness. Preferably, the first insulating film is formed so as to have a film thickness of 500 angstroms or less, 100 angstroms or less, or 50 angstroms or less.

More preferably, in the above-mentioned structure, a control gate for electrical field application is formed on the insulating film so as to face the channel region.

It is further preferable that the transistor, formed of the substrate and the semiconductor layer mentioned above, be a thin-film transistor (TFT). For example, the semiconductor layer is formed in a low-temperature polysilicon process, and the thin-film transistor is formed as low-temperature polysilicon TFT.

On the other hand, the manufacture of a thin-film semiconductor device according to the present invention includes a first step of forming a semiconductor layer, which has each source, channel and drain region on a substrate; and a second step of forming an insulating body, which has granular charge trapping bodies inside, to trap the charge of injected carriers.

In this case, it is preferable that the second step also have the steps of forming a first insulating film, constituting a portion of the above-mentioned insulating film, on the semiconductor layer; placing the granular charge trapping bodies on the first insulating film; and forming a second insulating film, constituting the remaining portion of the insulating film mentioned above, on the first insulating film with the charge trapping bodies being kept on the first insulating film.

Preferably, the first insulating film is formed by plasma oxidation. Additionally, as another preferred example, charge trapping bodies are formed by sputtering and etching. In this case, it is preferable that Al-Si be sputtered and

that only Al be etched thereafter. Moreover, according to another preferred example, the second insulating film is formed by the CVD method. Besides these methods, it is also possible to form the first insulating film by plasma oxidation, the charge trapping bodies by sputtering and etching, and the second insulating film by the CVD method.

Furthermore, the granular charge trapping bodies are, for instance, silicon particles.

Moreover, the first step is a step where the semiconductor layer is formed in a low-temperature polysilicon process. A low-temperature polysilicon TFT (thin-film transistor) may be formed in this step.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows an example of an electronic book using a liquid crystal display device with a built-in thin-film semiconductor device having memory functions in accordance with the present invention; FIG. 2 shows the electric block structure of the liquid crystal display device; FIG. 3 is a partial cross-sectional view, showing the thin-film structure of a TFT memory as a semiconductor thin-film device; FIG. 4 is a plane view of the TFT memory in FIG. 3; FIG. 5 shows the steps of manufacturing the TFT memory; and FIG. 6 is a figure, showing qualitative changes in the characteristics of the control gate voltage Vg and the drain current Id of the TFT memory in respect to information writing.

EMBODIMENTS

The preferred embodiment of the present invention is explained hereafter, with reference to the drawings.

The liquid crystal display device 1 according to the embodiment constitutes the electronic book shown in FIG. 1. This liquid crystal display device 1 has a book-form frame 1A and an opening and a closing cover 1B in the frame 1A. In frame 1A, a liquid crystal display unit 2 is arranged so as to expose a display surface at the surface, and a control unit 3 is also arranged.

As shown in FIG. 2, a panel 4 is arranged inside the frame 1A. On this panel, a picture element unit ia provided as the above-described liquid crystal display unit 2, and a scan driver 5 and a data driver 6 are provided to control the display of the picture element unit for each picture element. Also provided is a controller 7 for controlling displays through both drivers 5 and 6, and a memory 8 where display information is stored in advance. The controller 7 and the memory 8 are conventionally mounted on a separate panel from that of the display unit 2 and the drivers 5 and 6, but the controller 7 and the memory 8 are mounted on one panel 4 in the embodiments. The display body having this structure is generally known as a System on Panel.

Such a device may be provided by the application of a low-temperature polysilicon TFT (thin-film transistor). Specifically, to each memory element of the memory 8, a memory element using the low-temperature polysilicon TFT of the present invention as a thin-film semiconductor device (mentioned as TFT memory hereinafter) is adopted, instead of a conventional floating gate MOS or the like.

This TFT memory is explained below.

FIG. 3 shows a cross section of one element of a TFT memory 11 as a thin-film semiconductor device; and FIG. 4 shows the positional relations of electrodes when the TFT memory 11 is seen from the top.

The TFT memory 11, as shown in FIG. 3, has a glass substrate 21, and a source 22a, wherein a channel layer 22b and a drain 22c made of a polysilicon layer 22 are formed on one part of the substrate 21. An extremely thin first gate oxide film 23 is formed over the entire polysilicon layer 22. The film thickness thereof is, for example., about 50 angstroms. As other thicknesses, the first gate oxide film 23 may be 50 angstroms or thinner, 100 angstroms or thinner, or 500 angstroms or thinner; and preferably, the film is formed to be extremely thin.

On the first gate oxide film 23, silicon particles 24 for charge storage are deposited. Regarding the silicon particles 24, for instance, the particle diameter is about 100 angstroms and the density per unit area is about 20%. These particles may be composed of other materials, such as semiconductor particles or metal

particles. As for additional particle diameters, it is preferable to form the silicon particles 24 at a particle diameter of 1 μm or below, 1000 angstroms or below, or 500 angstroms or below.

A second gate oxide film 25 is formed while the silicon particles 24 are maintained on the first gate oxide film 23. The film thickness is about 1000 angstroms. A control gate 26 is formed on the second gate oxide film 25, at the location corresponding to the channel layer 22b. The electrode is made of polysilicon, or a metal such as aluminum or tantalum. Furthermore, a layer-to-layer insulating film 28 is formed over the entire element of the TFT memory 11. Additionally, as shown in FIG. 4, a source electrode 27S and a drain electrode 27D are formed through contact holes at appropriate locations from the source 22a and the drain 22c.

The method of manufacturing this TFT memory 11 is explained hereafter, based on FIGs. 5 (A) to 5 (D).

First, as shown in FIG. 5 (A), for example, a base film 21A made of SiO2 is formed on the top of the glass substrate 21; an amorphous silicon film is accumulated thereon; and e.g., an excimer laser is used to irradiate the amorphous silicon film, and crystallizes the film by locally heating and melting the film, thereby forming a polysilicon layer 22 patterned in a predetermined shape.

Subsequently, as shown in FIG. 5 (B), a first gate oxide film 23 is formed by plasma oxidation. The conditions of plasma oxidation are established so as to provide an extremely thin first gate oxide film 23.

Then, aluminum-silicon (Al-Si) is sputtered, and the aluminum is removed by wet etching. As a result, as shown in FIG. 5 (C), a plurality of silicon (Si) particles 24 remains on the first gate oxide film 23. The silicon particles 24 may be left only above the channel layer 22b.

With the silicon particles 24, SiO2 (silicon dioxide) is accumulated by the CVD method on the first gate oxide film 23, as shown in FIG. 5 (D), thereby forming a second gate oxide film 25. Accordingly, a second gate oxide film 25 is coated with the silicon particles 23 dispersed in an appropriate density on the first gate oxide

film, burying the silicon particles 24 in the insulating body.

Furthermore, though not shown in FIG. 5, a control gate 26 is formed by a conventional method (see FIG. 3). Subsequently, by the conventional method where ions are injected by using the control gate and a mask layer as masks, a source 22a and a drain 22c are formed in the polysilicon layer 22. Thus, the polysilicon layer 22 becomes the source 22a, the channel layer 22b and the drain 22c. Subsequently, a layer-to-layer insulating film 28 is formed over the entire TFT memory 11; and after the contact holes are formed, a source electrode 27S and a drain electrode 27D are formed (see FIG. 3).

In the manufactured TFT 11, the silicon particles 24 are completely covered with oxide films 23 and 25, so that the charge injected into these silicon particles 24 cannot easily escape, since the energy barrier between the silicon particles 24 and the oxide films 23 and 25 is substantial. In this state, information is written into the TFT memory 11.

When information is written into the TFT memory 11, an appropriate positive voltage is applied to the control gate 26, as shown in FIG. 7 (a), and electrons are injected into the silicon particles 24 from the channel side by "Fowler-Nordheim" tunneling. As the first gate oxide film 23 is formed of an extremely thin thickness, the injection of charge will be easy.

Therefore, the characteristics of the "control gate voltage Vg – drain current Id" of the TFT 11 qualitatively change, as shown in FIG. 6, in response to information writing. In the state before the information is written, electrons are not yet injected, and the threshold voltage is low. As electrons are injected by information writing, its charge is trapped and the threshold voltage increases, holding the information (charge) .

Additionally, when the information in the TFT memory 11 is erased, an appropriate positive voltage may be applied to the drain 22C, which is opposite to the writing process shown in FIG. 7 (b). However, in actually constructing a memory array, the transistors that form a switch for each memory cell are generally connected in series in order to provide selectivity.

As a memory element is formed by the application of the low-temperature polysilicon TFT, a System on Panel, such as that shown in FIG. 2 can be provided. Accordingly, the structure and the scale of a device or a system as a whole becomes compact, and maintenance and the like becomes easy. Additionally, as TFT memory, use may be made of the memory of an IC card and the like, broadening the range of applications.

Moreover, the charge trapping bodies buried in the gate oxide film (gate insulating film) of the TFT memory 11 are in granular form, so that there is no danger of a short-circuit between a source and a drain.

Furthermore, as the TFT memory 11 is formed of a low-temperature polysilicon TFT, economical glass substrates may be used.

Additionally, the present invention is not limited to the above-noted embodiments and may also be modified in various forms.

As explained above, the present invention has a semiconductor layer, which has each source, channel and drain region formed on a substrate, an insulating film formed on the semiconductor layer, and granular charge trapping bodies (for instance, a plurality of semiconductor or metal particles) inside the insulating film to trap the charge of injected carriers, so that TFT memory may be provided by adding memory functions with granular charge trapping bodies to a thin-film transistor (TFT) element comrising a substrate and a conductive layer.

As a result, the applications of TFT elements are broadened to memory elements. Conventionally, TFT elements are only applied to the picture elements of displays and the peripheral circuits. As the TFT memory is used as a memory unit, the unit may be mounted on the same panel as that of other thin-film structural bodies using TFTs (for instance, a liquid crystal display and the driver circuit thereof), thus significantly miniaturizing, compacting or making an energy-saving device and system.

Claims

1. A thin-film semiconductor device comprising a substrate, a semiconductor layer including a source region, a channel region and a drain region formed on the substrate, an insulating film formed on the semiconductor layer, and granular charge trapping bodies inside the insulating film to trap the charge of injected carriers.

2. The thin-film semiconductor device according to Claim 1, wherein the charge trapping bodies are a plurality of particles of semiconductor or metal.

3. The thin-film semiconductor device according to Claim 2, wherein the plurality of particles are silicon particles.

4. The thin-film semiconductor device according to Claim 3, wherein the silicon particles have a particle diameter of 1 μm or less, 1000 angstroms or less, or 500 angstroms or less.

5. The thin-film semiconductor device according to Claim 2, wherein the insulating film comprises a first insulating film formed on the semiconductor layer and a second insulating film formed on the first insulating film; and wherein the plurality of particles are located between the first insulating film and the second insulating film.

6. The thin-film semiconductor device according to Claim 5, wherein the first insulating film is formed in an extremely thin thickness.

7. The thin-film semiconductor device according to Claim 6, wherein the first insulating film is formed so as to have a film thickness of 500 angstroms or less, 100 angstroms or less, or 50 angstroms or less.

8. The thin-film semiconductor device according to one of Claims 1 to 7, wherein a control gate for electrical field application is formed on the insulating film facing the channel region.

9. The thin-film semiconductor device according to one of Claims 1 to 8, wherein the substrate and the semiconductor layer constitute a thin-film transistor

(TFT).

10. The thin-film semiconductor device according to Claim 9, wherein the semiconductor layer is formed in a low-temperature polysilicon process, and the thin-film transistor is formed as a low-temperature polysilicon TFT.

11. A method of manufacturing a thin-film semiconductor device comprising a first step of forming a semiconductor layer which has a source region, a channel region and a drain region on a substrate; and a second step of forming an insulating body, which has granular charge trapping bodies inside to trap the charge of injected carriers, on the semiconductor layer.

12. The method of manufacturing a thin-film semiconductor device according to Claim 11, wherein the second step comprises the steps of: forming a first insulating film, constituting a portion of the insulating film, on the semiconductor layer; depositing the granular charge trapping bodies on the first insulating film; and forming a second insulating film, constituting a remaining portion of the insulating film, on the first insulating film while the charge trapping bodies are kept on the first insulating film.

13. The method of manufacturing a thin-film semiconductor device according to Claim 12, wherein the first insulating film is formed by plasma oxidation.

14. The method of manufacturing a thin-film semiconductor device according to Claim 12, wherein the charge trapping bodies are formed by sputtering and etching.

15. The method of manufacturing a thin-film semiconductor device according to Claim 14, wherein the charge trapping bodies are formed by Al-Si sputtering and etching.

16. The method of manufacturing a thin-film semiconductor device according to Claim 12, wherein the second insulating film is formed by the CVD method.

17. The method of manufacturing a thin-film semiconductor device according to Claim 12, wherein the first insulating film is formed by plasma oxidation, the charge trapping bodies are formed by sputtering and etching, and the second insulating film is formed by the CVD method.

18. The method of manufacturing a thin-film semiconductor device according to

one of Claims 9 to 17, wherein the granular charge trapping bodies are silicone particles.

19. The method of manufacturing a thin-film semiconductor device according to one of Claims 9 to 18, wherein the first step is a step to form the semiconductor layer in a low-temperature polysilicon process, thus constructing the substrate and the semiconductor layer as a low-temperature polysilicon TFT (thin-film transistor).

ABSTRACT

A TFT memory 11 is provided with a polysilicon layer 22, wherein each region of the source 22a, channel the 22b and the drain 22c are formed on a substrate 21, and gate oxide films (insulating films) 23 and 25 are formed on the polysilicon layer 22; and a plurality of silicon particles 24 for trapping the charge of injected carriers are placed between the gate oxide films 23 and 25. Specifically, the gate oxide films comprise a first gate oxide film 23 and a second gate oxide film 25 formed on the first gate oxide film 23; the plurality of silicon particles 24 are located between the first gate oxide film 23 and the second gate oxide film 25, and the first gate oxide film 23 is formed in an extremely thin thickness.

Figure 4

FIG.1

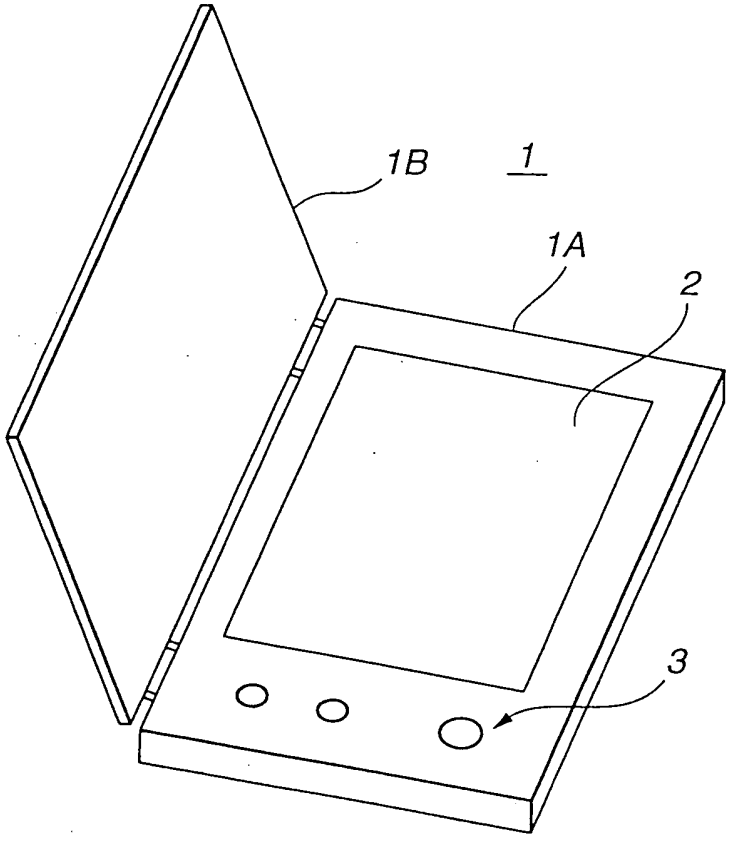


FIG.2

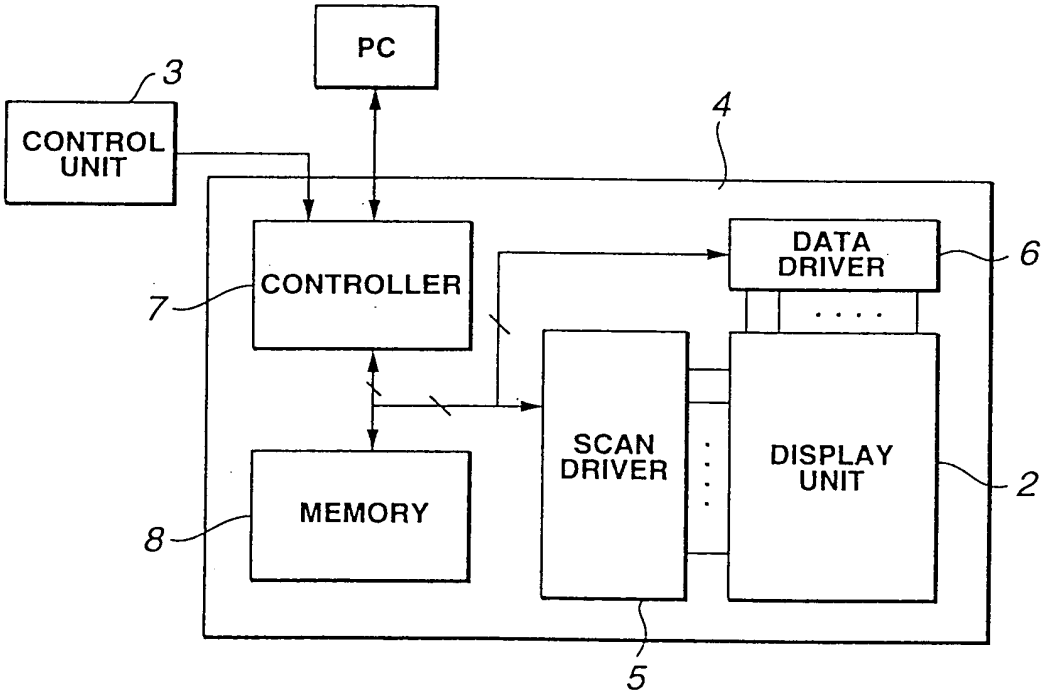

PC
3
CONTROL UNIT
4
CONTROLLER
7
DATA DRIVER
6
SCAN DRIVER
DISPLAY UNIT
2
MEMORY
8
5

FIG.3

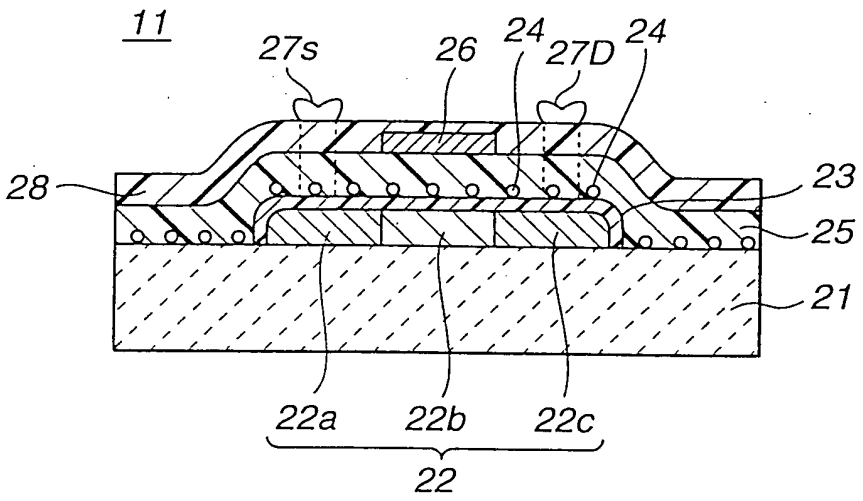


FIG.4

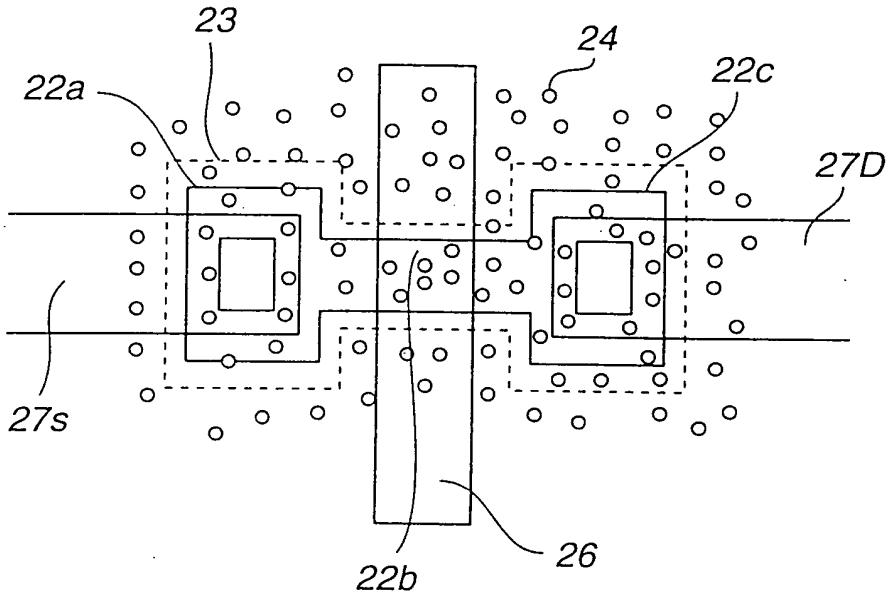


FIG.5A

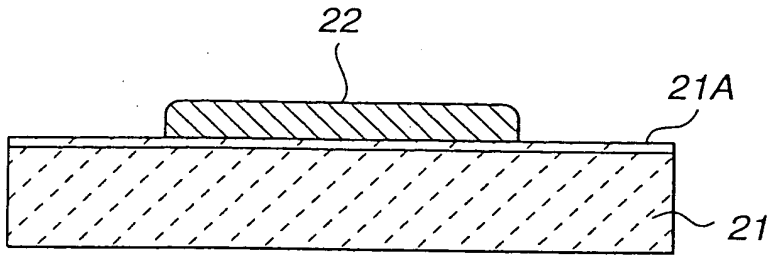


FIG.5B

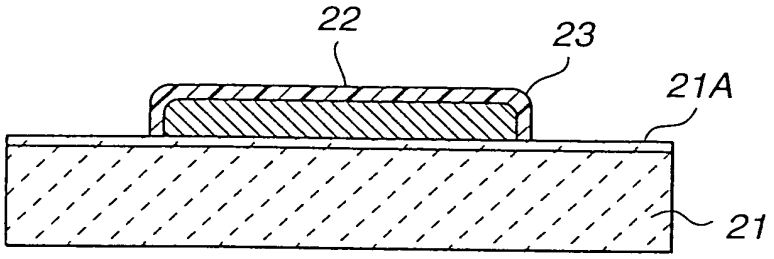


FIG.5C

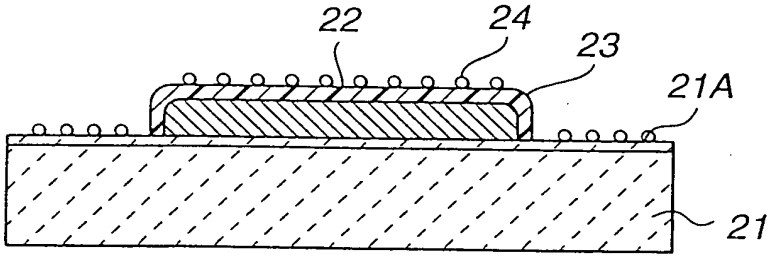


FIG.5D

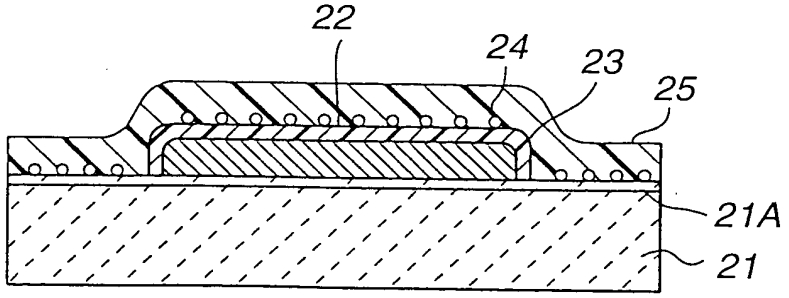
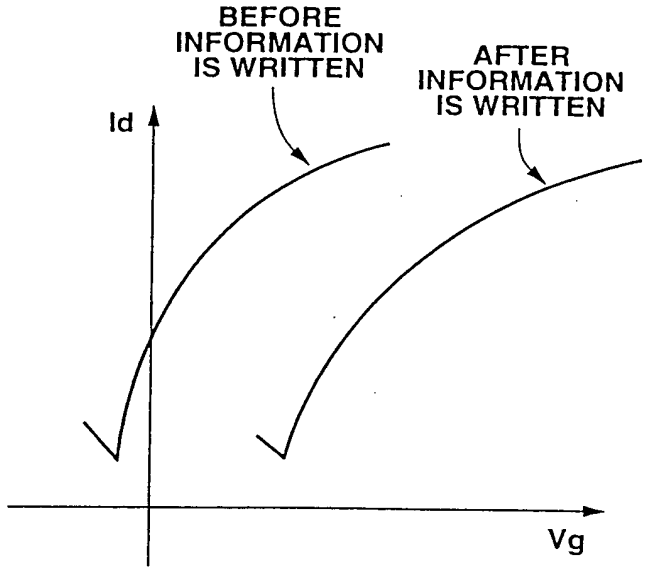


FIG.6


BEFORE
INFORMATION
IS WRITTEN
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Id
Vg

FIG.7A

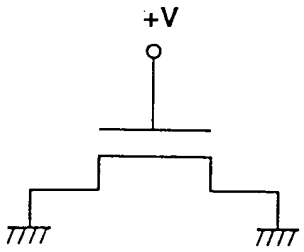

FIG.7B